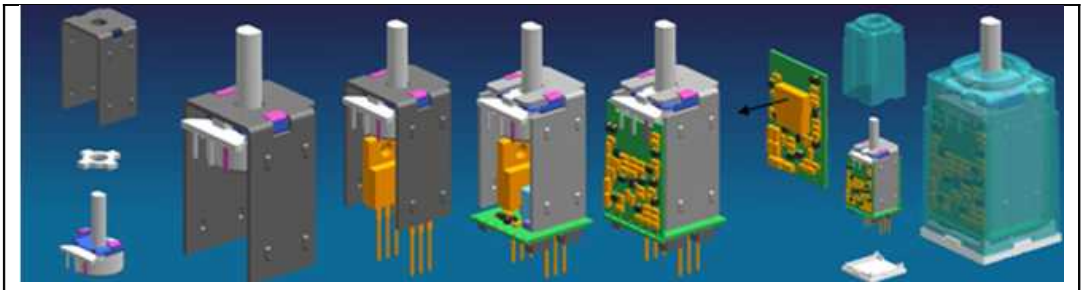
30 Mech Universal Dimmer Test Specification



30 Mech Universal Dimmer

1.Introduction

1.1.Scope

This document sets out the requirements to produce a new Finished Goods Tester to test the UNIVERSAL Dimmer Range of products from Clipsal.
The Tester will be commissioned at an EMS site, **most probable JABIL Shanghai, China.**
This dimmer is capable of working with loads up to 450 watts, the major difference between it and other dimmers is that it can detect what type of load is connected, and adjusts the type of phase control accordingly.

1.2.Revision control

Version	Date	Author	Description
1.0	11-Dec-2007	Kevin O'Brien	Originator
1.1	03-March-08	Kevin O'Brien	Updated to reflect what's happening: 1: Test one unit as opposed to 2 2: Update time line

1.3.Company Details

Name: **Clipsal Integrated System**

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Postcode: 518001.
Wedsite: www.clipsal.com/cis

Ordering & Invoice

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1.4.Contacts

Description	NAME	Function	Phone Number
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2.General

2.1.**Design**

- This Finished Goods test system is primarily designed to test two (2) type of product in a high volume, flexible manufacturing environment.
- The internal electronics is the same for both products; the only difference is the method of controlling the dimming, **the POT shaft are different**, so if we are to use automatic solution, the method needs to handle both shaft types.

Year / Qty	2008	2009	2010	2011
Clipsal Dimmer	40,000	130,000	320,000	400,000
PDL Dimmer	10,000	20,000	30,000	40,000

This table shows the expected numbers.

- The possibility of it testing similar type dimmers in the future is also possible, so additional fixtures that can be easily changed have to be designed.
- The current proposal is the tester has the ability to test ~~**TWO DUTs**~~ **ONE DUT** at the one time. ~~This will actually happen in serries as opposed to parallel.~~

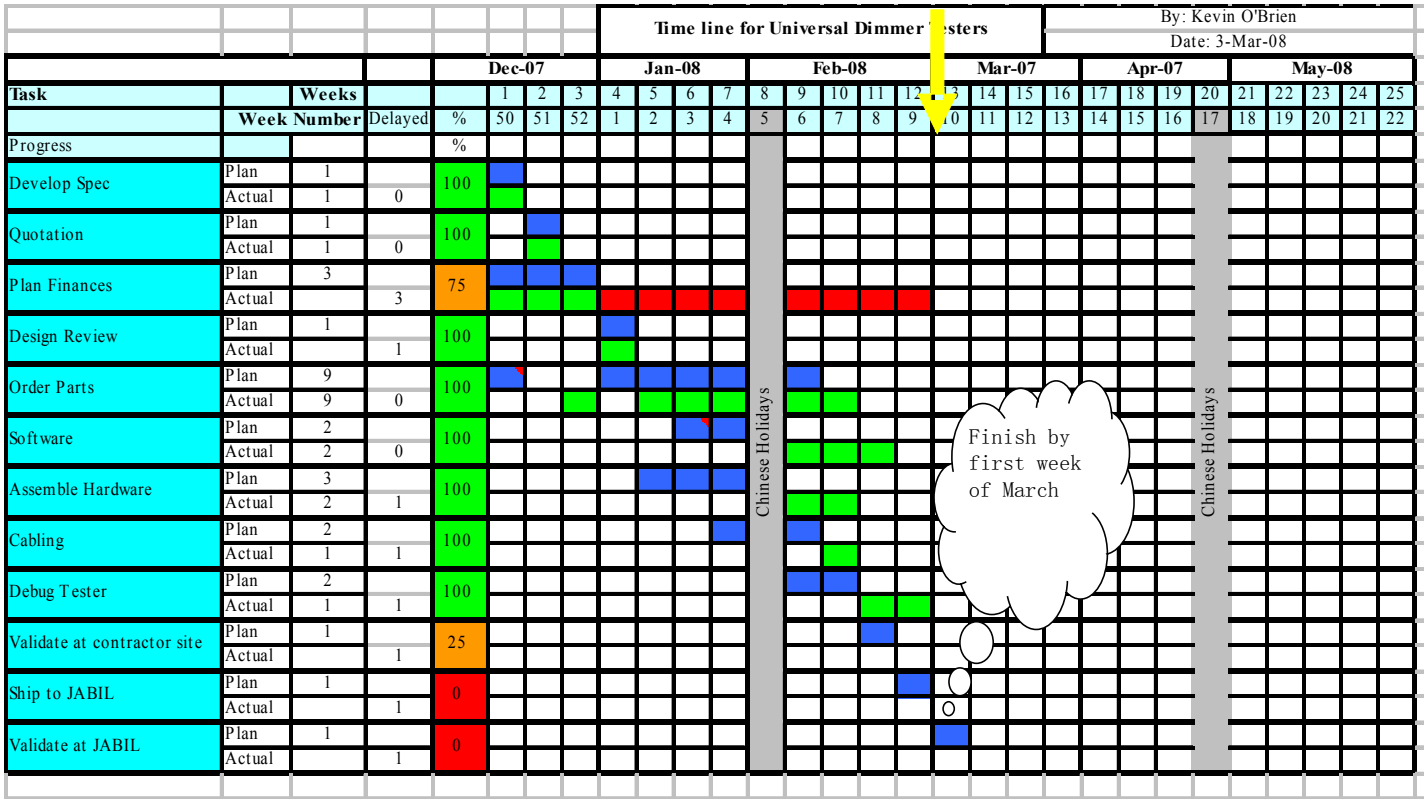
2.2.**System Operating Input Requirements**

- Mains supply: 1 phase.
- 10 – 100 BaseT LAN Network.

2.3.**Lead Times and Planning**

The following is a proposed time scale to complete the project, all will have to be verified and confirmed with the contractor.

Completion date expected to be no later than the **Week 10 of 2008**



2.4.**Quote and Payment**

- As part of the quoting process, the quote should contain the following information:
  - The price of each instrument. (Includes or excluding VAT)
  - The price of additional hardware, cable, relays, cabinet, etc…
  - The labour cost to put together the tester.
  - The price of the fixtures and jigs.
  - The price of developing the software.
  - Taxes.
  - Terms of payment.
  - Warrant agreements.

- Terms of payment: (To be confirmed with contractor)

2.5.**Confidentiality**

- All design work will be the property of Clipsal Shenzhen, hardware and software.
- The contractor will have to sign a Non Disclosure Agreement with Clipsal before any further documentation is handed over.
- A contract will have to be signed by both parties before any work begins.

3.Product to be tested

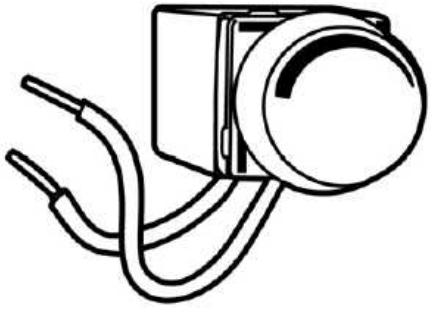
3.1.**Objective**

The main objective of the tester is provide a solution that allows the 30 Mech UNIVERSAL Dimmer to be tested at a Finished Goods level, thus allowing a reduced set of test at PCBA level at the EMS site.

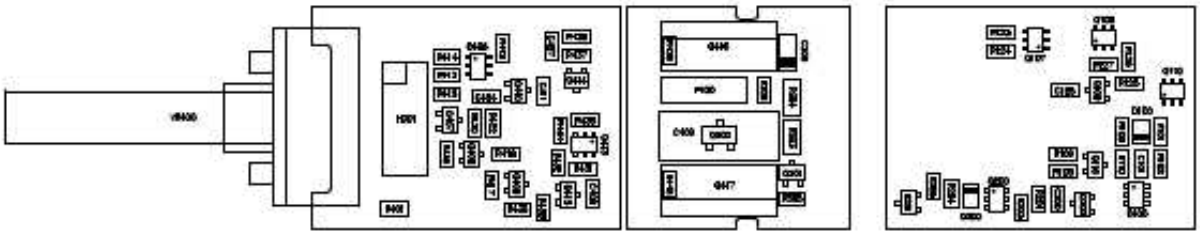
The following a list of test to be carried out, a more detailed Test Specification will be supplied.

Test	**Method of measuring**
Measuring conduction angles	The current waveform will be obtained from current sense transformers connected to each load, with 100W load connected. This waveform will be connected to an Analogue Input (Differential Mode) of the DAQ card, where the waveforms can be analysed. Expected results **1ms to 10ms, 30mV to 500mV peak**. (Both polarities), high sample rates are not required. Go to Appendix A to view expected signal.
Rise and Fall times	The voltage across the LOAD need to captured this time. The Current waveform could also be used for this. Different loads will have to be switched in to get product to operate as leading or trailing edge. Because of resolution of DAQ card, only one signal can be analysed at the time, so this part done in series. High sample rate, 1million +. Expected results, **10µs to 50µs, 30mv to 500mV peak.** (Both polarities) Go to Appendix A to view expected signal.
Short circuit protection	A load capable of driving the product into "short-circuit" will be switched in series with the DUT. The product should shut down. Expected currents to flow if there is a problem: **10A to 20Amps at 240V**. The program needs to take into account if the DUT fails, i.e. big currents flow for a long time, the program need to stop this situation.
ZeroXing measurement	Source voltage compared with the current waveform. An alternative way to do it would be to use the trigger out from the AC source to know when the source voltage crosses Zero. Expected reading of **+/300µs.** View expected Signal
Over voltage Clamping test	The AC source, HP 6812B can be used to put a spike on the 240 volts output. This spike should be enough to put the product into an over voltage condition. If DUT went into an OV condition, than a current should have flowed through the load.
TrimPOT control	A method need to be developed to know where the DUT is at as regards minimum and maximum settings.
Thermal Testing	Research the option to add thermal testing on the heatsink, so a thermal device touches the heatsink and checks the result. This would happen at the very end of the test, once both DUT have been on for at least one minute.
DC Current measure 0-50mAmps	Need to measure DC current through the DUT, could use the DMM or else Hall Effect Transducer.

3.2. UNIVERSAL Dimmer Mechanism



PRODUCT OVERVIEW	
Dimmer Type	Universal
Load Rating	450W
Compatible Load Types	All
Casing Type	Existing Mechanism Casing
Maximum Grid Capacity	3 Dimmers per Plate (+3 separate switches)



This drawing shows the three different PCBs connected together to produce the finished product. One PCB is for Leading Edge, the second for Trailing, and the third contains the power devises and the power supply

The products are intended to dynamically sense the connected load type, and utilise either Leading Edge or Trailing Edge Phase Control to achieve dimming, as appropriate to the connected load(Resistive, Inductive, Capacitive Load Type)
This dimmer is capable of working with loads up to 450 watts, the major difference between it and other dimmers previously produced by Clipsal is that it can detect what type of load is connected, and adjusts the type of phase control accordingly. It can switch from Leading edge dimming to Trailing edge dimming, depending on the nature of the load connected, thus improving EMC emissions from the product.

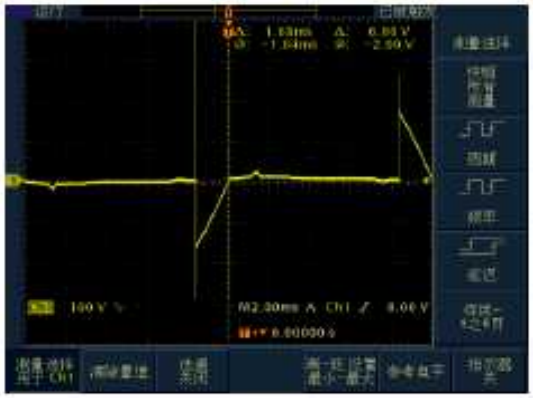


Figure 5 The waveform of output at minimum brightness

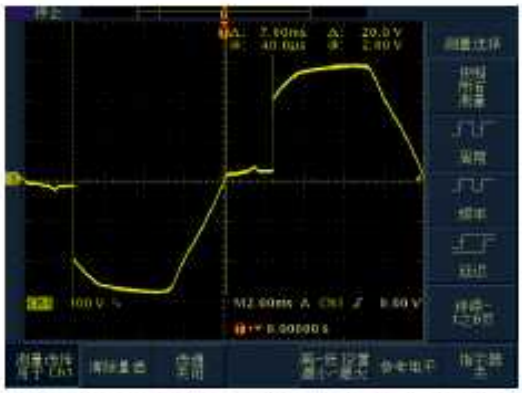


Figure 4 The waveform of output at maximum brightness

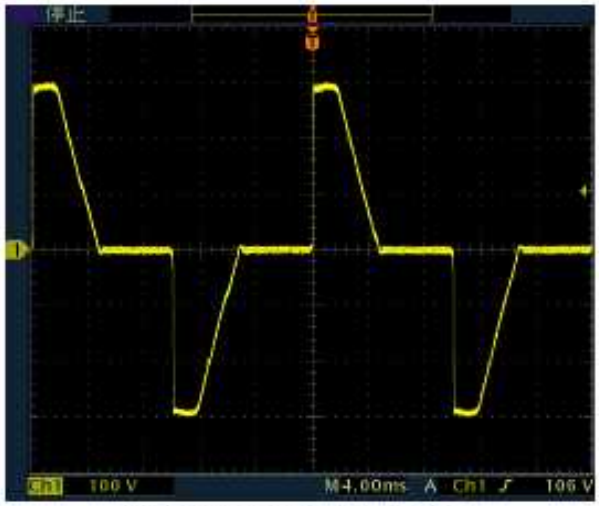


Figure 1 Leading edge mode voltage wave

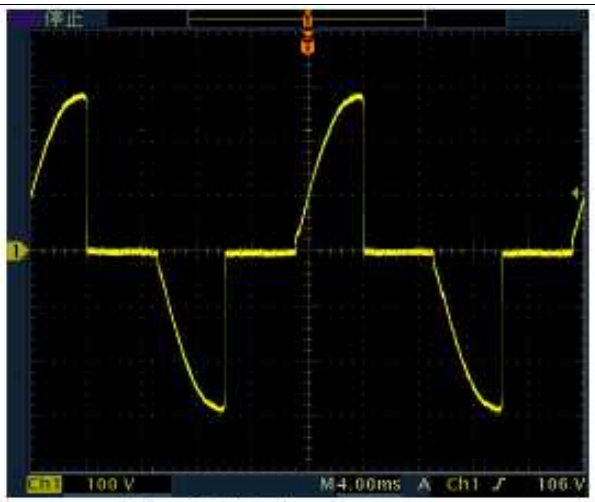


Figure 2 Trailing edge mode voltage wave

These are typical signals to be measured, except these are of voltage across the DUT, we will use current sense transforms in series with the DUT.

4.Design Overview

4.1.Objectives

The broad objectives for modern manufacturing test are highlighted below, followed by the intended means of achieving them in the proposed test rack design

	OBJECTIVE	ATE SOLUTION
1.	Measure the required test parameters in a reproducible and repeatable manner.	Instruments run under computer control.
2.	Conduct all the test (& programming) steps in the correct order.	Programmed "Test Sequence" for each product variant.
3.	Effective control of test acceptance limits.	Programmed test limits set by test developer.
4.	Minimise the risk of operator-induced errors occurring during set-up and operation.	Set-up and reading of instruments handled by computer control.
5.	Efficient use of high value test & measurement equipment.	Test instruments mounted in common use "test rack". Interchangeable test fixture concept to connect instruments to product.
6.	Maximise test throughput.	Provide parallel test facilities where practical.
7.	Minimise effect of test system on product function.	Use high quality instruments and up-to-date test and measurement practices.
8.	Minimise the risk of injury to operating and maintenance staff.	Design to guidelines AS 4024.1-1996 'Safeguarding of machinery".
9.	Minimise test system footprint.	Use compact "state-of-the-art" test instruments where possible.
10.	Minimise system downtime attributable to breakdown maintenance and repair.	Use readily available commercial test instruments where possible.
11.	Record test results and data in a convenient and foolproof manner.	Electronic logging of results to disk or network.
12.	Identify product test status in a convenient and foolproof manner.	Provide facility to implement automatic PASS marking (Fixture dependent).

4.2.**Safety**

This item comprises a number of aspects:

- ***Fire hazard***
  - Fire hazards emanating from test equipment are minimised by specifying approved commercial test instruments from reputable manufacturers.
  - Custom circuitry shall be designed and constructed to withstand worst-case conditions, which could occur, such as PC controller lock-up or a completely faulty (short-circuit) product under test (DUT).
  - The design specifies two (2) custom built passive (fixed) load banks that may dissipate up to 1750W (total worst case). Being relatively light in weight, these units shall be mounted near the top of the tester immediately adjacent to the main rack exhaust fans. They shall be mounted so as to ensure an adequate air flow through each load bank.
  - In the unlikely event that an internal over-temperature event does occur, series connected temperature cut-out switches shall be fitted to the system to shut off all system power.

- ***Electrical Safety***
  - Electric shock hazard during testing
    - The system supplies isolated, synthesised 300VAC levels to the device under test.
    - A system will have to be developed where the operator never has access to live mains. This can be achieved by using magnetic safety switches on the enclosure.
  - Electric shock hazard during maintenance

Incoming "Supply side" electrical connections shall be housed in their own separate DIN rail enclosure to prevent accidental contact with high current circuitry and ensure segregation from control wiring. Electrical wiring to be performed to AS/ NZS 3100:2002 or similar.	 Fig 1 shows an example of such a housing

    - The rack/cabinet shall be provided with lockable doors, which will be locked during normal production use. Access keys are to be held by authorised technical personnel only.

5.Electrical specification

5.1.General

oWhenever possible Clipsal/Schneider Relays/Contactors and the like should be used over the competitor's brands. If alternatives need to be used, it should be OKAY with Clipsal first.

oA connector panel with all of the relevant connectors will be made available to allow quick and easy removing the fixtures.

oThe connector panel will have the following signals available on it:

- o24 DIO
- oPower supplies→ +12Volts @ 1Amp, +5Volts @ 1Amp, +24Volts 2 1Amp.
- o8 Relay Drivers → +12Volts @ 100mAmps.
- o2 Differential Analogue Inputs.
- oLive, Neutral and Ground.
- o2 Loads, ability to test 2 universal dimmers.
- oSpare connections on power connector, to allow for future unforeseen work.
- o4 DMM switched measurements points.

oThere could be high currents flowing through the tester for a period of time, so the type of cable and connectors used need to well over-rated for the current specified.

oThe fixtures must also have probes that can at least handle 10 Amps or more.

o

oEach DUT will have a 6 Amp MCB in serries with it, so these MCBs need to easily accessible to the operator in case they trip because of faulty products.

oThe relays need to be at least 10 Amps and good quality, and easy to change if need be.

oFor future design reasons, the tester needs to be able to accommodate for testing of four (4) DUTs at the one time. So a DAQ card with at least 32 Analogue Input lines, and a DIO with 96 bi-directional lines.

oFor the above reasons, enough free space needs to be made available for further expansion.

- 30% free space for future development

5.2.**Wiring**

- All wiring must be labelled and a schematic with the matching labels supplied.
- The following is colour coding for the cable to be used.

WIRING COLOUR CODES FOR TEST EQUIPMENT		
	WIRE COLOUR	**WIRE SIZES ***
		Choose a wire size at least twice the current rating if the Power Supply. E.G. 5V@1A, choose 16/0.2 3Amp wire.
DC VOLTAGES:		
0V	BLACK	7/0.2, 16/0.2, 24/0.2
+5V	RED	7/0.2, 16/0.2, 24/0.2
+12V or +15V	ORANGE	7/0.2, 16/0.2, 24/0.2
-12V or -15V	PURPLE	7/0.2, 16/0.2, 24/0.2
+24V	YELLOW	7/0.2, 16/0.2, 24/0.2
AC VOLTAGES:		
EARTH	GREEN/YELLOW or GREEN	24/0.2, 32/0.2
NEUTRAL	BLUE	24/0.2, 32/0.2
ACTIVE	BROWN	24/0.2, 32/0.2
LOAD	WHITE	24/0.2, 32/0.2
OTHERS:		
DIGITAL/LOGIC	GREY	
ANALOGUE SIGNAL	WHITE or SHIELDED CABLE	7/0.2, 16/0.2, 24/0.2
	or MULTICORE CABLE	7/0.2, 16/0.2, 24/0.2
C-BUS SUPPLY	WHITE/BLACK	16/0.2, 24/0.2
SHIELDS/BRAIDS	BLACK	
(NOTE: Where shield/braid is to be connected to 0V or GND. Unplait (or "COMB-OUT") shield/braid and twist strands together, use at least half of the circumference (cut any remaining braid level with outer sheath). Cut twisted braid to approx.15mm from where outer sheath has been removed, solder wire to shield/braid and connect other end of wire to the 0V or GND point).		

6.Hardware Specification

6.1.**Objective**

This section explains the hardware, and what are the expected outcomes.

6.2.**Physical Layout**

- The physical layout of the tester has not been defines, so it will be the job of the contractor to come up with some proposals, where a number of different options can be given to the customer, and then a decision will be made as to what's the best solution.
- But the expectation is a tabletop format, with the necessary instruments loaded under the table, and control/switching and safety circuits on both sides, both lockable cabinets.
- The positioning of the fixtures and jigs must be so that the operator will never come in contact with live mains during test, so this involves some form of safety, when the lid is open then mains is removed from all jigging.

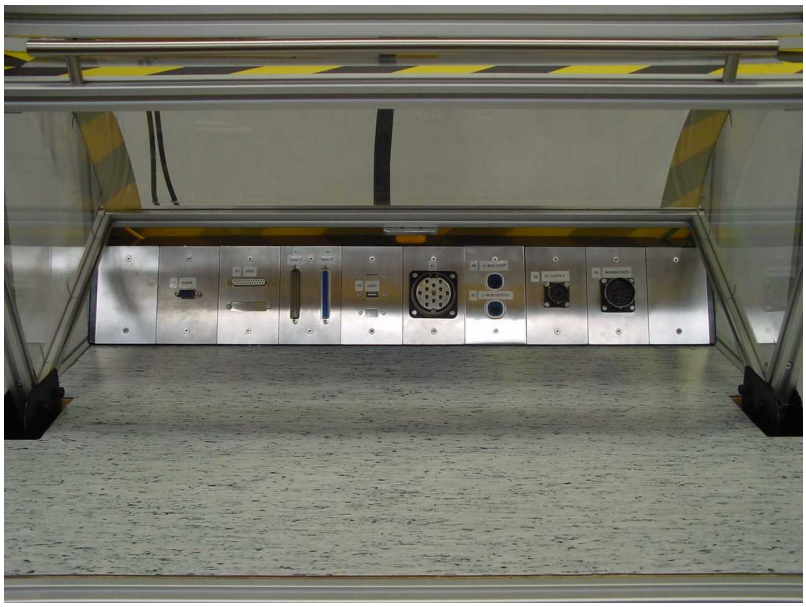


Fig 1, The connector panel could look something like this

6.3.**Instruments to be used**

The following is a list of hardware expected to be used in the system.

Qty	Part No	Supplier	**DESCRIPTION**
1	NI-6254	NI	DAQ card, 32 Analogue inputs, minimum of 1.25M samples per second
1	NI- 6509	NI	DIO CARD, 96 bi-directional DIO.
1		TBD	Industrial PC with accessories (monitor, keyboard, scanner or barcode reader etc)
1		Agilent	AC source, 750 watts, HP6812B
1		TBD	Digital Multi Meter capable of capturing a wave (1000 VDC)
1 1			Relay Driver circuit. Servo Motor Driver/Stepper motor or Motor with torque control

6.4.**The Fixtures**

The following is the requirements for the fixtures.

- Wherever large currents could flow, then the correct or over rated probes and cables should be used. (10 Amps or greater)
- The DUT must be easy to connect to the jig, no opportunity to get it wrong, Poka Yoke.
- The fixture will then be connected to the "back plain" using suitable connectors, most probably Harting connectors for the power, as there could be 10 amps flowing through the cables at worst case situation.
- The fixtures should be easily to replace as this tester could be used in the future for similar product testing, again Poka Yoke, the operator can not plug the fixture in incorrectly..
- The fixture will also need to contain the method of rotating the Trim POT shaft.
- The fixture will need a method for Auto Pass Marking. Only if the DUT passed the test must it be marked, this could possibly be an engraver type instrument.

7.Software Specification

7.1.**Objectives**

- The objective is to develop a Test Sequence, drivers/components and a user interface all developed, LabView is the preferred language. (Test Stand with Test Stand is also an option)
- The Operator Interface must be developed in such a way that the operator cannot make mistakes easily.
- **Data recorded on each measurement, limits and result, and date and time of test. Final information about each DUT status after test, like; test time, operator tested, overall result, Pass/Fail or abort, or error, test stage it failed on, and failed result.**
- Expected Test Times per DUT should be less than 30 seconds.
- A log kept of any errors occurred during testing.

7.2.**Tasks to be done**

Main Tasks	Sub Tasks
Operator Interface	
	User friendly screens to instruct Operator on next instruction.
	A sequencer to ensure all test are carried out in an orderly fashion on each DUT in the fixture, DUT sensing used to determine this.
	Clear information on present and previous DUT status, pass/fail serial numbers, etc.
	Ability to select different products
Instrument Drivers	
	AC source
	DIO Card (Power Relay, Pneumatics, Auto Pass Mark & General house keeping duties)
	DMM
	DAQ Card
	Safety Control
Data Storage	
	Develop what we want to store
	Parallel Testing
	Build Header information
	Collect results on two Hard Drives
TARS	Description of what JABIL and TARS file will be provided later

7.3.**Deliverables**

The Sequencer:

- It is expected that the sequencer will run through each step in an orderly fashion.
- The option to select different products to be tested, (2 different sequences so far)
- The operator will have very little interaction with the DUT, it will all be done automatically.
- The following information should be made available to the user:
  - The status and serial number of the last DUT tested. (Green=PASS, RED=FAIL)
  - If a DUT failed, what stage did it fail at.
  - Test times and a rolling averages
  - The status of the current DUTs being tested.
  - An abort soft button, which will finish testing as soon as possible, (not continue testing).
  - The ability to view past number of DUTs tested & and failed data if applicable, possible as an extra Tab, just load results into a table, and the table just roles the old results off.

Components must be developed for each instrument and service provided to be easily reused. The components must be developed in such a way that all of the following criteria are met:

- Each component can be tested on it's own, it does not need any other code to get it to function correctly.
- A debug screen should be supplied with each component, allowing it to be tested for correct operation, debug or calibration purposes; this debug screen should be easy to use.
- Built in help should outline what services the component will provide, and clearly explaining all inputs and outputs.
- The default input setting on the GUI should be set such that without changing anything, the component will work first time, no errors.
- Each component should be able deal with it's own errors.

Other requirements:

- The limits of each test must NOT be hard coded into the application; preferably limits could be stored in a text file separate from the code.
- Expected test time for each DUT will be around 30 seconds +/- 10%. (But with the option to leave on for longer time).
- The operator needs to be able to easily identify which DUTs passed and which DUTs failed the test, to ensure that faulty product does not get past the tester.
- Serial number of each DUIT to be recorded and test results of each test and status. (Pass or Fail).
- Auto Pass Marking control, something like punch as opposed to drill, because to drill the heatsinker might have some trouble with designee.
- All source code to be supplied to CIS.
- All source code is the property of Clipsal, Shenzhen.
- The ability to be able to turn ON and OFF TARS from the GUI.
- The ability to be able to test one DUT at a time as opposed to two, JABIL will need such a feature because if doing repair, they will not want to test two DUT together only one.

8.Documentation

8.1.Documentation supplied by Schneider Electric

The following is a list of documents, which will be supplied to the contractor to enable them to complete the job, the schematics will be in Protel format, and the layouts are drawn in AutoCAD.

Item	Document number	Description
1	Block Diagrams	Block Diagrams of Tester PDF or Visio.
2	Test Requirements	Test Specs for UNIVERSAL Dimmer, also expected test times.
3	Qualification Plans	A set of rules that the tester must achieve. For Example: FPY > 99% on known good product, the ability to detect faulty product, and acceptable test times.

8.2.Documentation supplied by contractor

Item	Document Description	Comment
1	Wiring schematic in Protel	
2	Wiring list in Excel	
3	Parts list of tester and parts sourced	
4	Maintenance Manual	
5	Each Test Sequence documented	
6	User Manual	

9.Acceptance

9.1.Universal dimmer Mechanism Test

A qualification plan will have to be developed to validate each part is working as expected.
Once the tester has passed the qualification plan, it will be deemed to be accepted by Clipsal.
A Qualification Plan will be carried out by trained Clipsal staff in accordance with Schneider policy.
No Fault Found, (NFF) must be less than 2% or FYP greater than 98% if testing all good product.

10.Improvements/Different From E84 Bench

10.1.Hardware

- We don't need the PWM signal at the dimming is controlled by TrimPOT.
- Load Box on top of bench as opposed to inside tester, makes it easier to change lamps and debug if need be.
- Load Box don't need to have connectors on them, they can be hardwired as part of the tester.
- The light visible from each load, but not too bright, so some diffuser in front of hole, so no need for the LEDs on the front of the tester to show which load is on.
- Electrical access from the back, do not put all control and relays in one box.
- Some kind of cover on the AC source.
- DCmA measurement, to measure DC current drawn by DUT.
- We will test two at the one time, but in serries, not in parallel, so initially turn on both, with 400 Watt loads, then start testing one of the units, if alls OK, leave it on while testing the other unit. Then start testing the other unit, then at the end, just a quick verify that the first unit is still working, by checking the current waveform.
- Added a step to try Thermal Testing of the HeatSink to see if the Power devices are connected.
- Add Clipsal Relay Matrix, PTB09, which is a 16 to 1of a 2 wire MUX, would make it easier to have extra measurement if required.
- Keep 500 watt Halogens below the 300 watts & the 150 Watts, just so the heat does not heat up the 500 Watts for short circuit testing, (The 500 Watts have lower resistance while cold).
-

10.2.Software

- DIO Driver should be easier to understand.
- DAQ driver easier to understand
- TARs files required.
- Turn ON/OFF TARS.
- The software has to handle two DUTs, if one fails what happens, etc.. so a bit more complex.
- Expect at least two trips to Shanghai, one to commission & the other in case of warranty job.
- View past serial numbers tested.
- Test one or two DUT, driven by a software switch.

10.3.Spare Parts supplied

One or more of each part spare that has the potential to break, like servo motors, relays, lamps, and any other mechanical parts that could wear easily
If any special PCBAs are to be made, also spare for this..

11.Appendix

11.1.Definition of Terms

DUT →	Device Under Test.
NI →	National Instruments
TS →	Test Stand
LV →	LabView
TBV →	To Be Verified
DAQ→	Data Acquire

11.2.**Test Requirements**

This file contains the first draft of the test requirements from engineering.

Universal Dimmer Mechanism – Production Testing Regime (Draft 2)

Production testing of the Universal Dimmer Mechanism essentially involves verification of the main circuit functional mechanisms.

Several different load types are required to be switched in series with the dimmer circuit in order to test dimmer operating modes.

Test Equipment:

Mains Power Source

- 230V/50Hz ac (and capable of 100Hz dc i.e. full-wave rectified sinusoidal waveform) non-inductive voltage source with low transient impedance (i.e. $R_s \leq 0.1\Omega$ and peak half cycle surge current capability ≥ 75A)

Trailing Edge Test Load

- Nominal 100W @ 240V incandescent lamp ($35\Omega \leq R_{Cold\ Filament} \leq 45\Omega$)

Leading Edge Test Load

- Partially Inductive load comprising 2.5mH ± 10% air-core inductor in series with nominal 100W @ 240V incandescent lamp filament (Filament resistance @ 25°C within the range of $35\Omega \leq R_F \leq 45\Omega$).

"Short-Circuit" Test Load

- Resistive Load; $R_L = 3.3\Omega$, 100W, 10% with peak power rating of 15kW, in series with 6A MCB, or
- Lamp filament load comprising 1500W @ 240V halogen lamp ($2.5\Omega \leq R_{Cold\ Filament} \leq 3.5\Omega$) or equivalent

High Inductance Test Load

- Iron Core Ballast Inductor; L = 1H ± 10%, $25\Omega \leq R_{COIL} \leq 35\Omega$, typically used as a ballast in 36W fluorescent lamp fitting

Over Temperature (Batch Test) Test Load

- Nominal 600W@240V incandescent lamp (i.e. 3 x 200W@240V incandescent lamps)

Explanation Notes:

- The "Short-Circuit" resistive test load must be robust incase of failure of the D.U.T where full mains voltage may be momentarily applied to the load – until activation of series connected MCB.

1. Trailing Edge Mode Tests

Minimum Conduction Angle (nominal 2.0ms)

- Verification of correct conduction timing at minimum setting.
- Verification of correct low pass filter timing delay – confirms mains ripple immunity function.

Conditions:

- D.U.T control potentiometer rotated fully anti-clockwise
- D.U.T line & load terminals connected in series with a 230V/50Hz ac voltage source and the Trailing Edge Test Load

Requirements:

- Load CURRENT waveform conduction period within range: $1.5ms \leq t_C \leq 2.5ms$
- Commencement of load current relative to line voltage zero-crossing is within range: $-0.3ms \leq t_{ZC} < +0.3ms$

Load Voltage Transition Time (Steady State) (nominal 30us @ Φ_C = 2.0ms)

- Verification of correct switching transition time – necessary for overall efficiency and EMC performance

Conditions:

- As per test no 1.1
- Steady state operation of D.U.T and load is achieved (i.e. operational time exceeds one second)

Requirements

- Load voltage waveform trailing edge transition time (90% - 10%) within range: $20\mu s \leq t_f \leq 40\mu s$

Maximum Conduction Angle (nominal 8.0ms)

- Verification of correct conduction timing at maximum setting

Conditions:

- As per test 1.1 but with D.U.T control potentiometer rotated fully clockwise

Requirements:

- Load current waveform conduction time within range: $t_C \geq 7.5ms$
- No visible flicker on the lamp load

2. "Short-Circuit" Cutout Function

2.1 Short Circuit Test in Both Mains Polarities

- Verification of protective cutout function at short-circuit events

Conditions:

- D.U.T control potentiometer rotated fully clockwise
- D.U.T line & load terminals connected in series with a 230V/100Hz dc voltage source and the "Short-Circuit" Test Load

Requirements:

- After application of supply voltage of each polarity, steady state rms load current is within range: $I_{LOAD} \leq 10mA$

2.2 Optional Short Circuit Test

- Verification of protective cutout function at short-circuit events

Conditions:

- D.U.T control potentiometer rotated fully clockwise
- D.U.T line & load terminals connected in series with a 230V/50Hz ac voltage source and the Trailing Edge Test Load
- "Short-Circuit" Test Load connected in parallel with the Trailing Edge Test Load with the ability to be switched in and out
- The "Short-Circuit" Test Load is switched in after steady state operation of the D.U.T and Trailing Edge Test Load is achieved

Requirements:

- After application of the "Short-Circuit" Test Load, the Trailing Edge Test Load is off

3. Leading Edge Mode Tests

3.1 Minimum Conduction Angle (nominal 2.0ms)

- Verification of ability to detect lightly inductive loads i.e. iron-core LV lighting transformer loading
- Verification of correct conduction timing at minimum brightness setting

Conditions:

- D.U.T control potentiometer rotated fully anti-clockwise
- D.U.T line & load terminals connected in series with a 230V/50Hz ac voltage source and the Leading Edge Test Load

Requirements:

- Load current waveform conduction period within range: $1.5ms \leq t_C \leq 2.5ms$

3.2 Load Terminal Voltage Transition Time (nominal 20µs @ $\Phi_C = 2.0ms$)

- Verification of correct switching transition time necessary for overall efficiency and EMC performance

Conditions:

- As per test no. 3.1

Requirements:

- Load terminal VOLTAGE waveform leading edge transition time (10% - 90%) range: $15\mu s \leq t_f \leq 30\mu s$

3.3 Maximum Conduction Angle (nominal 8.0ms)

- Verification of correct conduction timing at maximum brightness setting
- Verification of correct low pass filter timing necessary for mains ripple immunity function in LE mode

Conditions:

- As per test no. 3.1 but with D.U.T control potentiometer rotated fully clockwise

Requirements:

- Load current waveform conduction time within range: $7.5ms \leq t_C \leq 8.5ms$

4. Over-voltage Clamping Test (nominal 500V)

- Verification of surge voltage protective clamping function
- Verification of highly inductive load detection mechanism – necessary for product operation with neon transformer & fan motor loads

Conditions:

- D.U.T control potentiometer rotated fully clockwise
- D.U.T line & load terminals connected in series with a 230V/50Hz ac voltage source and the High Inductance Test Load

Requirements:

- Peak voltage developed across D.U.T terminals, corresponding to MOSFET turn-off transitions while D.U.T is initially in trailing edge mode, is clamped to less than 500V
- Average DC current through D.U.T is below 5mA

5. Over Temperature (Batch Test) - Optional

- Verification of over load thermal wind-back function
- Test to be performed on a to be determined sample size of a production run

Conditions:

- D.U.T control potentiometer rotated fully clockwise
- D.U.T line & load terminals connected in series with a 230V/50Hz ac voltage source and the Over Temperature (Batch Test) Test Load

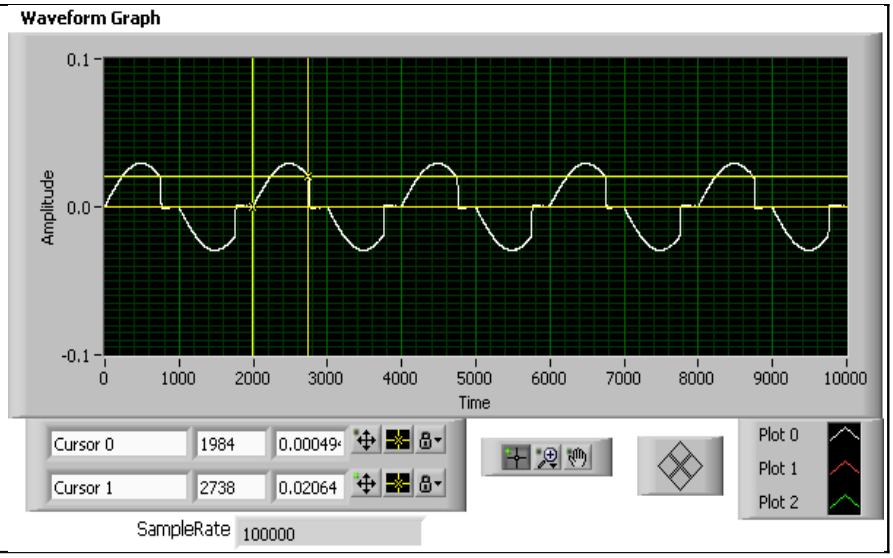
- D.U.T to be covered by a plastic box (i.e. 56E1 enclosure) - helps to speed up the test
- D.U.T left running for ½ an hour

Requirements:

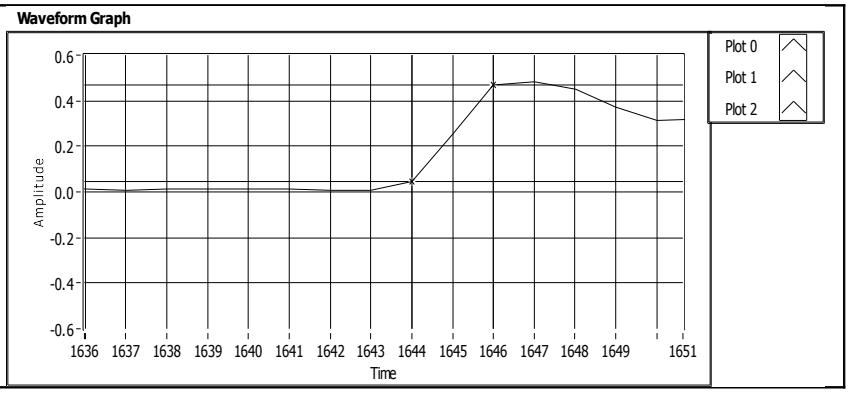
- After ½ an hour, load current waveform conduction time within the range of: $t_C \leq 5.0ms$

11.3.**Signals to be measured:**

Conduction measurement signals

This shows the type signal that needs to be measured. Typical results would be 1ms to 8ms, about 30mVolts. Both cycles need to be verified.	

Rise and fall times at different points in the test

This shows a typical rise time of leading edge dimmer products. Expected results 10µs to 50µs. Again 30mVolts	

Voltage Zero Crossing

Commencement of Load current relative to line voltage zero-crossing is within range. Expected results +/-300µs.